REMARKS/ARGUMENTS

Prior to this amendment, claims 1-15, 20-34, 36 and 37 were pending. In this amendment, no claims are amended, canceled, or added. Thus, after entry of this amendment, claims 1-15, 20-34, 36, and 37 remain pending.

Rejections under 35 USC § 103(a), Leaver in view of Cong

Claims 1-9, 20-28 and 36-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Leaver et al. (US Patent No. 6,195,788) in view of Cong et al. ("Cut Ranking and Pruning: Enabling a General and Efficient FPGA Mapping Solution").

Claims 1-15

Claim 1 is allowable over the cited references, either alone or in combination, as those references fail to teach or suggest all the elements of claim 1. As Leaver is directed to finding a mapping of a user design to reconfigurable logic, and not determining a usage of fixed-configuration secondary hardware, there are many differences.

I. A netlist is not actual hardware on a device

For example, claim 1 recites "*a plurality of programmable logic elements, each comprising reconfigurable logic hardware and fixed-configuration secondary hardware.*"

At pages 2 and 8, the Office Action asserts that the registers and I/O ports of the netlist are the "*fixed-configuration secondary hardware.*" *See Leaver*, col. 7 lines 44-51. Here, Leaver is talking about elements (e.g. a register) of a netlist. A netlist is a software representation of a circuit. The actual hardware used is different than the elements of the netlist. *Id.*, col. 7 lines 26-34. Thus, the registers and I/O parts that are discussed for the logic cone of the netlist are not actually hardware of the target device, but are part of the user design. In contrast, claim 1 recites "*each comprising reconfigurable logic hardware and fixed-configuration secondary hardware.*"

If the Examiner still believes that these registers and I/O ports are indeed hardware on a device, Applicants respectfully request an identification of the user design. Applicants also request clarification of what the reconfigurable logic hardware and the programmable logic elements are asserted to be.

II. Leaver's anchors have an input and an output, not a plurality of inputs

As another example, claim 1 recites "*the fixed-configuration secondary hardware having a plurality of inputs.*"

At page 2, the Office Action asserts that Leaver's recursion to a next node coupled to the anchor teaches the above claim element. *Id.*, col. 9 lines 28-35. The next node may be the one input or the one output for the anchor. However, there is no mention of an anchor having more than one input. Also, FIGS. 4A-4C show only one input into each anchor.

Accordingly, Leaver, alone or in combination with Cong, does not teach or suggest "*the fixed-configuration secondary hardware having a plurality of inputs,*" as recited in claim 1.

III. What are the programmable logic elements and their common inputs?

As another example, claim 1 recites "*the inputs common to at least two of the programmable logic elements.*"

As previously mentioned, it is unclear what is being asserted as the programmable logic elements. Therefore, it is also unclear of what are the inputs that are common to at least two of the programmable logic elements. Note that these inputs need to be into the asserted fixed-configuration secondary hardware.

Accordingly, these references do not teach or suggest "*the fixed-configuration secondary hardware having a plurality of inputs, the inputs common to at least two of the programmable logic elements,*" as recited in claim 1.

IV. Leaver's connectivity diagram shows a same input to two anchors, not multiple assignments of inputs to the same anchor

As another example, claim 1 recites "*for each of a plurality of portions of the user design, determining one or more sets of input assignments to the fixed-configuration secondary hardware, each set providing an implementation of that portion of the user design using the fixed-configuration secondary hardware.*"

At page 8, the Office Action mentions that the I/O ports can be fixed-configuration secondary hardware, and that the connectivity diagram shows multiple inputs

assignments to an I/O port. *Id.*, col. 7 lines 55-60. The connectivity diagram shows one same logic signal from node 304 being sent to two I/O pins, both marked 302. *Id.*, FIG. 3. Thus, multiple input assignments are not given to one fixed-configuration secondary hardware.

At page 3, the Office Action also points to the creation of logic cones as teaching determining input assignments to the anchors (asserted fixed-configuration secondary hardware). *Id.*, col. 9 lines 19-25 and 60-67. The creation of logic cones determines which nodes are grouped into which cones. The input to an anchor does not change in this process. The logic cones are a way of partitioning the netlist, not rearranging or re-assigning inputs to different anchors.

Accordingly, these references do not teach or suggest "*determining one or more sets of input assignments to the fixed-configuration secondary hardware*," as recited in claim 1.

V. Leaver compares cost of PTERM v. LUT, not ranking input assignments

As another example, claim 1 recites *"ranking the input assignments by determining a number of times each of a plurality of signals in the user design is assigned as a respective input to the fixed-configuration secondary hardware*."

At page 8, the Office Action asserts that the connectivity diagram (FIG. 3) teaches ranking input assignments. *Id.*, col. 7 lines 55-60. This section mentions that a netlist can be depicted graphically. There is no mention of ranking anything at all.

At page 3, the Office Action reiterates that table 1 teaches ranking the input assignments. *Id.*, col. 10 lines 1-15 and 41-64. However, as outlined on page 10 of the last response, this section details the cost of using PTERM vs. LUT. The relative costs are not ranked, and Applicants have been unable to identify any relevancy of the cost ratio to different input assignments to fixed-configuration secondary hardware.

Accordingly, these references do not teach or suggest "*ranking the input assignments by determining a number of times each of a plurality of signals in the user design is assigned as a respective input to the fixed-configuration secondary hardware*."

VI. Cong ranks cuts based on a smaller mapped area, not input assignments

As another example, claim 1 recites "*selecting the highest ranked input assignment, where a first signal in the plurality of signals in the user design is assigned as a first input to the fixed-configuration secondary hardware more than any other signal in the user design is assigned to an input to the fixed-configuration secondary hardware.*"

Cong ranks cuts based on optimization objectives, such as area minimization. *See Cong*, section 3.2.

At page 9, the Office Action asserts that the decomposition of Cong teaches that the logic cones with a greater number of nodes are ranked higher. *Id.*, section 3.3.5. However, this statement is the opposite of what occurs in decomposition.

"Decomposition can provide more freedom in forming different LUTs at the cost of more cuts to be enumerated." *Id.*, section 3.3.5. Since the number of cuts increases, the size of a logic cone decreases. Thus, even if the size of logic cone meant there were more registers, the number of registers would be decreasing. Note that the ranking mentioned in this section is just that different size LUTs may be used on an FPGA.

Additionally, at page 9, the Office Action states that ranking a cut by the number of nodes contained within it is the same as ranking an input assignment based on the number of registers in the group, citing to ¶ 41 and table 5 of the present specification. The ranking of cuts is still not relevant to the ranking of input assignments to fixed-configuration secondary hardware. Even if Cong did rank cuts by size, the size is not related in any way to the number of registers whose secondary hardware has a particular input assignment.

Accordingly, Cong does not teach or suggest this claim element.

Claim Rejections under 35 USC § 103(a), Leaver, Cong, Wallace

Claims 10-15 and 29-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Leaver et al. in view of Cong and in further view of Wallace (US Patent No. 7,020,855). These claims respectively depend upon allowable independent claims 1 and 20, and are thus allowable. Note that the cited teachings of Wallace fail to make up for the deficiencies in Leaver and Cong.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance and an action to that end is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 415-576-0200.

Respectfully submitted,

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